



COMPOUND SEMICONDUCTOR

CONNECTING THE COMPOUND SEMICONDUCTOR COMMUNITY

TACCOTA

**HIGH TEMPERATURE
AND CORROSION
RESISTANT COATING**



NIPPON KORNMEYER
CARBON GROUP



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Unconventional crystallinity

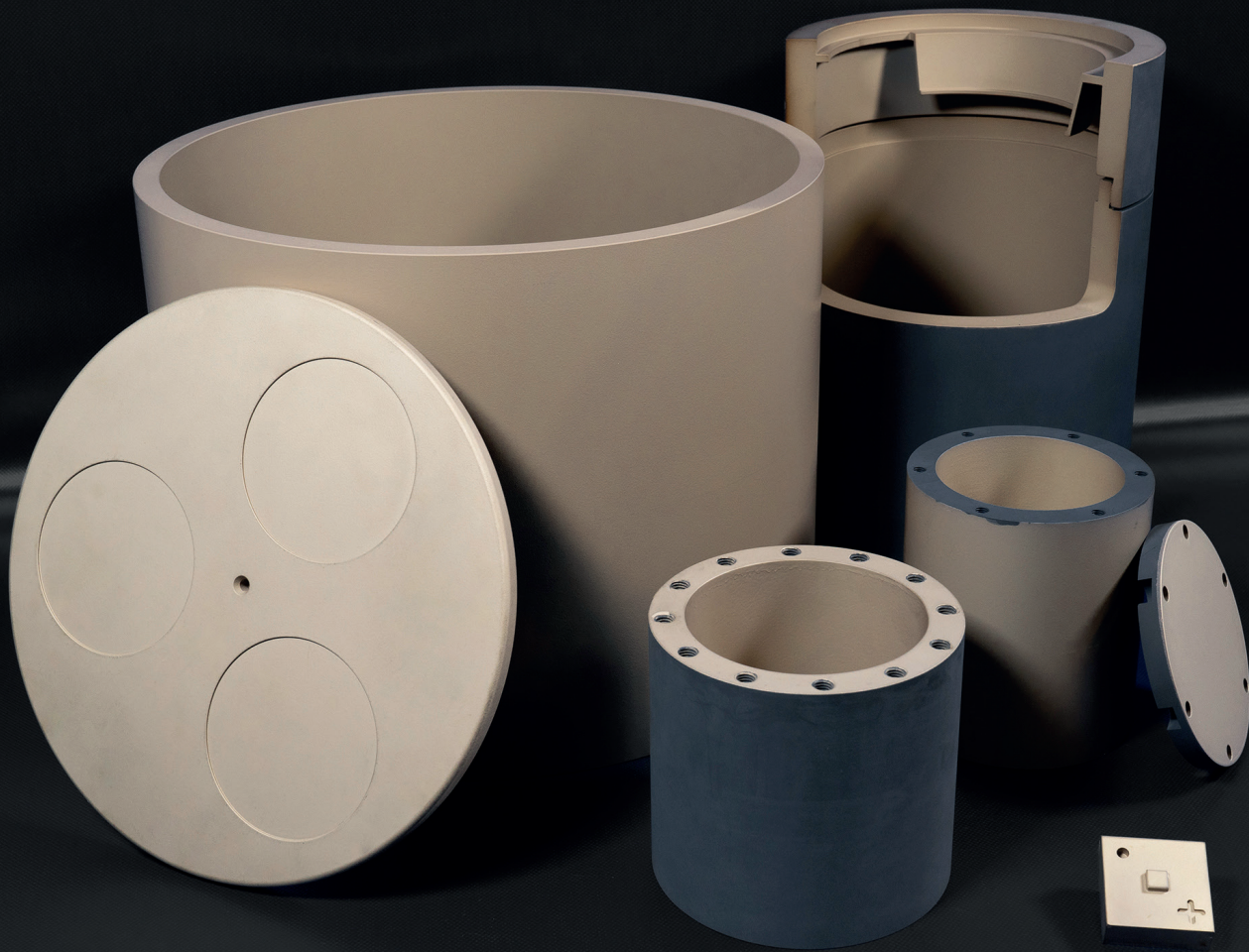
Cubic GaN promises to
address the low efficiency of
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Integrated tuneable laser
assemblies offer wide tuning,
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A novel form of Schottky diode

Reliable and efficient, the
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Coating at its best

Spraying graphite parts with tantalum carbide cuts the cost of producing SiC crystals and epilayers

**BY CHRISTIAN REIMANN, MATTHIAS TREMPA, KEVIN SCHUCK AND
MICHAEL LANG FROM FRAUNHOFER IISB, AND TORSTEN KORNMEYER AND
DIRK MUETZENICH FROM THE NIPPON KORNMEYER CARBON GROUP**

THE SEMICONDUCTOR INDUSTRY is booming, with one prime example the field of SiC power electronics. Here many high-volume fabs are either under construction or expansion, to support an increase in the production of SiC devices, which are being deployed in electric vehicles.

While every boom offers a great opportunity to increase profits, it also brings its own unique challenges. Crucial to ramping global SiC chip production is the manufacture of high-quality SiC crystals, wafers and epitaxial layers. In this context, it is crucial to consider the role of semiconductor-

grade graphite materials, which are used in the equipment that enables the growth of SiC crystals and the deposition of SiC epitaxial layers. Graphite, which is valued for its thermal insulation capabilities and inertness, is the preferred material for crucibles and susceptors in crystal-growing systems, and for planetary discs and satellites in epitaxial systems.

Killer degradation...

The production of SiC crystals involves harsh process conditions. The total corrosion of a graphite crucible may occur after just a few processes, due to temperatures of over 2000 °C and extremely

corrosive gas species that contain silicon. For instance, the production of SiC epitaxial layers involves: process temperatures that peak at 1600 °C; the combination of silane and propane, which are responsible for the growth of the SiC layer; and hydrogen and in some cases hydrochloric acid. The latter two can be used as carrier gases, or for very corrosive etching.

As well as simply eating up the graphite components, the harsh process conditions alter the emissivity and morphology of the component surfaces. This is a significant issue, severely impairing the reproducibility of the production processes and in turn having an impact on the resulting process stability – and thus the material quality of the SiC crystals and epitaxial layers. Another major drawback is that the harsh conditions can cause free carbon and carbon particles to be released from the corroded graphite parts, threatening the production of high-quality SiC semiconductor material.

Due to these considerable concerns, process engineers tend to only use these heavily stressed components a few times, and sometimes just once. It is a constraint that causes consumable material graphite to contribute significantly to the manufacturing costs of SiC crystals and epitaxial layers.

...and graphite shortages

It's of little surprise that graphite is in great demand in many sectors, due to its desirable physical and mechanical properties and its capability to form a wide range of geometries. Unfortunately, today's graphite industry cannot keep pace with the strong expansion plans of the global SiC industry, and competition between end users for the best possible supply of graphite is already underway. Fortunately, there's a game-changing solution that kills two birds with one stone. It's the introduction of protective layers, which tackle both the degradation of graphite parts and the graphite delivery shortage. It's a most welcome introduction, given the drastic increase of lead times for graphite components, driven by the booming semiconductor sector.

Today, protective coatings based on tantalum carbide (TaC) are already in use. The merits of this material include a melting temperature of over 3800 °C and a very good chemical resistance to reactive gases. Up until now, the approach to producing state-of-the-art TaC protective coatings is to use Chemical Vapour Deposition (CVD) to deposit this material on graphite components, a process that produces semiconductor-clean and gas-tight layers with a thickness of typically up to 35 µm. However, there are disadvantages of this technology, with the main drawbacks including high manufacturing costs, and once again, long delivery times. In addition, there are material issues, with cracks appearing through 100 percent dense crystalline TaC layers during repeated heating and cooling of the

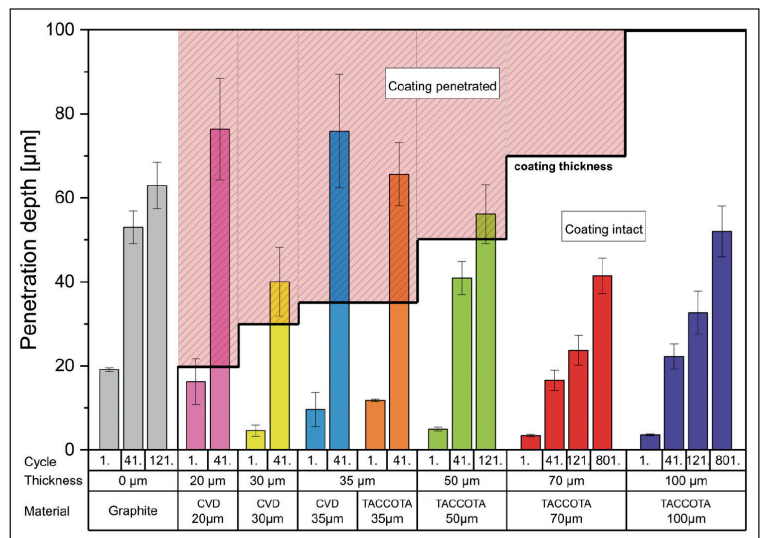


➤ Figure 1. The TaC process technology developed at Fraunhofer IISB allows adjustment of desired coating properties, such as thickness, shown here in the range 35 µm to 110 µm.

components. These cracks expose the underlying graphite, which strongly degrades over time and has to be replaced.

The spray solution

Motivated by addressing all these shortcomings, those of us at Fraunhofer IISB started to develop a disruptive coating technology more than five years ago, with the aim of compensating for the disadvantages of the state-of-the-art approach. We began with very simple laboratory-scale tests, involving the coating and evaluation of graphite shards.



➤ Figure 2. Scratch test results of Tacotta spray coating with variable thicknesses versus CVD TaC coatings performed after DIN50324 / ASTM G99 and G133. These results reveal an enhanced wear resistance due to increased coating thickness.

Over the years, our TaC coating technology has grown out of its children's shoes. Helping on this front has been the feedback from potential end users – it has been key to the further development of our technology. Today, our patented approach combines a water-based spray coating with subsequent temperature treatment. One great asset of our technology is that it is incredibly flexible when it comes to coating components of different sizes and geometries. Unlike CVD deposition of TaC, partial coating and component refurbishment is also possible. What's more, our technology is environmentally friendly, easy to industrialise, and free from conflicting materials.

We have evaluated the properties of our TaC coating. It is resistant to temperatures of more than 2500°C and corrosive gases. The thickness of the coating is variably adjustable in the range of 20 µm to 200 µm (see Figure 1), ensuring protection impact for extremely lengthy process times and a high number of cycles. Another benefit of our technology is that it produces TaC coatings with tremendous mechanical stability, thanks to interlocking with the



► Figure 3. SiC wafer carrier before (right) and after (left) several standard SiC epilayer processing runs.

underlying porous graphite. We have demonstrated this attribute with so called scratching-tests (see Figure 2).

Following two years of pre-development, we shared the potential of this newly developed technology with a number of investors. Our technology

Proven coatings

To investigate the contamination that results from a TaC coating during real application conditions, a case study has been performed at Fraunhofer IISB using a single-wafer SiC epitaxy reactor. For this purpose, semiconductor grade epi-ready SiC wafers have been processed at typical growth conditions – such as 1600 °C, and reactive gas flows of hydrogen, silane and propane – using a mean time for the growth of the SiC epi-layer of around 1 hour. For each run a virgin SiC wafer has been used and analysed at the upper surface (silicon side) by vapor phase decomposition, inductively coupled plasma mass spectrometry. This form of spectrometry determines the contamination level.

The first experiment involved three subsequent epitaxial runs and a virgin CVD TaC-coated setup. For this experiment, the set-up included a wafer carrier, which is directly in contact with the lower SiC wafer surface, and a susceptor chamber where the wafer carrier is embedded. Measurements show very low contamination levels for almost all measured elements for all three runs (see the figure above and to the right for contamination levels on the wafer surface). However, the surface contamination with tantalum coming from CVD TaC is initially quite high, and still at high values of more than $5 \times 10^{10} \text{ cm}^{-2}$ after the third run.

	Epi-Run	#1	#2	#3	#10	#11	#12	Ref.	Ref.
Detection limit (dl)	Susceptor	CVD TaC	CVD TaC	CVD TaC	TACCOTA	TACCOTA	TACCOTA	Unused SiC wafer	Industry Epi reactor (CVD TaC)
	Wafer carrier	CVD TaC #1 (1 st use)	CVD TaC #1 (2 nd use)	CVD TaC #1 (3 rd use)	TACCOTA #2 (1 st use)	TACCOTA #2 (2 nd use)	TACCOTA #2 (3 rd use)		
0.065	Li	<dl	<dl	<dl	<dl	<dl	<dl	<dl	n.m.
0.371	Na	<dl	<dl	4.536	1.199	<dl	3.750	1.068	n.m.
0.198	Al	2.570	<dl	<dl	<dl	1.213	4.155	<dl	n.m.
0.265	K	<dl	<dl	1.889	0.847	<dl	3.183	0.364	0.053
0.158	Ca	<dl	0.282	0.275	4.850	1.766	<dl	18.78	<dl (0.05)
0.125	Ti	<dl	<dl	<dl	0.229	<dl	0.664	<dl	<dl (0.03)
0.164	V	<dl	<dl	<dl	<dl	<dl	<dl	<dl	<dl (0.02)
0.431	Cr	<dl	0.490	<dl	<dl	<dl	<dl	<dl	0.105
0.124	Mn	<dl	<dl	<dl	<dl	<dl	<dl	<dl	0.488
0.375	Fe	<dl	2.575	<dl	<dl	<dl	<dl	<dl	0.306
0.062	Co	<dl	<dl	<dl	<dl	<dl	0.265	<dl	<dl (0.02)
0.783	Ni	1.456	<dl	<dl	<dl	<dl	<dl	<dl	<dl (0.25)
0.551	Cu	<dl	<dl	<dl	<dl	<dl	<dl	<dl	<dl (0.14)
0.206	Zn	<dl	<dl	0.233	0.178	0.075	0.150	<dl	<dl (0.05)
0.976	As	<dl	<dl	<dl	<dl	<dl	<dl	<dl	<dl (0.21)
0.015	Sr	<dl	<dl	<dl	<dl	<dl	<dl	<dl	<dl (0.003)
0.026	Cd	<dl	<dl	<dl	<dl	<dl	<dl	<dl	<dl (0.004)
0.007	Ba	<dl	<dl	<dl	0.180	0.234	0.128	0.051	<dl (0.001)
0.002	Ta	119.0	71.98	5.101	26.67	5.977	0.269	0.066	0.058
0.010	Pb	<dl	<dl	<dl	0.022	<dl	<dl	<dl	<dl (0.002)
0.037	Bi	<dl	<dl	<dl	<dl	<dl	<dl	<dl	<dl (0.001)

► Values for surface contamination in $1 \times 10^{10} \text{ cm}^{-2}$, measured by vapor phase decomposition, inductively coupled plasma mass spectrometry on the silicon side of epi-ready SiC wafers. Each run has used a virgin cleaned SiC wafer.

These results have been compared with those obtained with a virgin Taccota set-up. In this case, the initial tantalum contamination is around 75 percent lower, and after three runs it is below $0.3 \times 10^{10} \text{ cm}^{-2}$, a much more acceptable level. This low ground level of contamination has been observed for the other measured elements.

This study demonstrates that Taccota is ready for semiconductor application from a contamination point of view, opening the door to real application tests at the sites of manufacturers of SiC devices.

impressed the Nippon Kornmeyer Carbon Group (NKCG), a joint-venture between the German-based Kornmeyer Group and Nippon Carbon Japan. They have licensed our technology from Fraunhofer IISB and produced TaC-coated graphite parts for their customers. Our collaboration, which started in 2021, immediately bore fruit. Already, the reusability of our TaC coating for the the production of SiC crystals has been successfully demonstrated several times. In addition to this valued reusability for SiC epitaxy, we have shown that there is no contamination from the TaC layer, and that the processed SiC wafers are free from any surface contamination (see Figure 3 and the text box “Proven coatings”).

We have even demonstrated that the tantalum contamination that occurs during epitaxy on SiC wafers with virgin TaC-coated graphite components is reduced by 75 percent in the first processes, compared with state-of-the-art CVD coatings. Thanks to this, our technology enables longer production campaigns with one graphite setup.

The uptake of the TaC coating technology, which we refer to as Taccota, has increased following its proven success in PVT and the epitaxial SiC crystal growth process. The management of NKCG is investing in a significant increase in production capacity along the entire value chain, from CIP feedstock to the TaC-coated finished parts, and it is also funding the introduction of an industry-leading quality control and management system. This investment is enabling NKCG to address the demand of graphite in this massive market, and fulfil its long-term strategic growth plan, together with its cooperation partner Fraunhofer IISB.

Carbon: The power to materialise the future



NIPPON KORNMEYER
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Since 1968, the Kornmeyer family has been supplying and innovating the carbon-based materials market. Today Nippon Kornmeyer Carbon Group (NKCG) is a company jointly operated by the shareholders of Kornmeyer Carbon Group GmbH in Germany and Nippon Carbon Co. Ltd. In Japan, a Tokyo stock exchange listed carbon manufacturer.

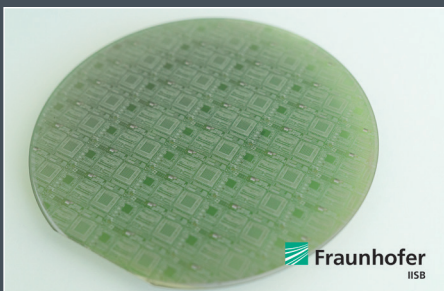
NKCG specializes in design and modelling, manufacturing, purification and several kinds of surface coatings, as well technical support of carbon-based and other ceramic materials. Decades of experience in the semiconductor industry, and material know-how combined with scientific expertise, enables NKCG to be a reliable partner along the entire process chain.



Intelligent Power Electronic Systems and Technologies

According to its motto, the Fraunhofer Institute for Integrated Systems and Device Technology IISB, founded in 1985, conducts applied research and development for the direct benefit of industry and society.

With scientific expertise and comprehensive systems know-how, IISB supports customers and partners worldwide in transferring current research results into competitive products, applied e.g. in electric vehicles, aviation, production, and energy supply.



➤ Fully processed 150 mm 4H-SiC High Temperature CMOS Wafer. Credit: Elisabeth Iglhaut, Fraunhofer IISB

The institute consolidates its activities in the two major business areas of Power Electronic Systems and Semiconductors. In doing so, it comprehensively covers the entire value chain from basic materials to semiconductor device, process, and module technologies to complete electronics and energy systems.

As a unique European competence center for SiC, IISB is a pioneer in the field of protective coatings like TaC, as well as SiC for graphite parts used in semiconductor materials production and processing.



➤ Fraunhofer IISB develops power electronics for the mobility sector, such as converters and e-drives for various types of vehicles all the way to components for the charging infrastructure. Credit: Kurt Fuchs, Fraunhofer IISB.